Quantum with Unity Pro
140 ERT 854 10
Time Stamp Module
User's manual

September 2004

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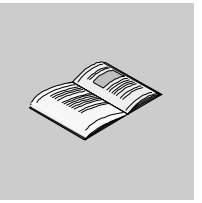
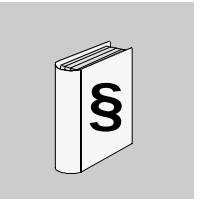


Safety Information



Important Information

NOTICE

Read these instructions carefully, and look at the equipment to become familiar with the device before trying to install, operate, or maintain it. The following special messages may appear throughout this documentation or on the equipment to warn of potential hazards or to call attention to information that clarifies or simplifies a procedure.

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DANGER

DANGER indicates an imminently hazardous situation, which, if not avoided, **will result** in death, serious injury, or equipment damage.

WARNING

WARNING indicates a potentially hazardous situation, which, if not avoided, **can result** in death, serious injury, or equipment damage.

CAUTION

CAUTION indicates a potentially hazardous situation, which, if not avoided, **can result** in injury or equipment damage.

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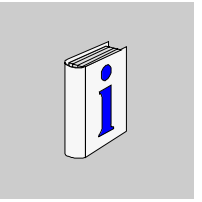
About the Book



At a Glance

Document Scope

This document describes the functionality and performance scope of the Time Stamp Module 140 ERT 854 10. It should show you how to provide your Quantum with time stamped data.

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Function Overview

I

Introduction

Overview

The first part of the manual for the intelligent input module 140 ERT 854 10 gives an overview of the structure of the module, the functionality and shows typical applications.

What's in this Part?

This part contains the following chapters:

Introduction

1

Module Overview

Overview

The 140 ERT 854 10 is an intelligent 32 point input module for Quantum that allows full configuration of inputs and evaluates the input signal status every 1 millisecond. Up to 9 ERTs can be installed on a local or remote module rack can be used.

The inputs

The 32 inputs are designed for input voltages of 24 to 125 VDC and are distributed in 2 independent groups. Each group is supplied with a separate external reference voltage (typically 24, 48, 60 or 125 VDC), to influence the threshold limit and minimum current consumption. The module status Ready, Active and Error as well as the input status (status of the terminals) are clearly displayed by the status LEDs on the module.
140 ERT 854 10 firmware processes inputs in four separate configurable function blocks with 8 inputs which support the following functions that can be selected.

- Binary inputs: input values are sent cyclically to the PLC.
- Event inputs: Time registered event logging for 1, 2 or 8 processed inputs, with 5 byte time register, integrated FIFO buffer for 4096 events and acknowledging PLC transfer by the user.
- Counter inputs: 32 bit addition of processed events up to 500 Hz that are transferred cyclically to the PLC.

Parameters can be set for processing individual inputs: (disabled, inverted, and with debouce filter). A configurable chatter filter can be activated for the event and counter inputs and event edge monitoring carried out.

Time synchronization

The module clock requires a time synchronization signal and provides a 24 VDC input with potential isolation for the following standard time receiver with DCF 77 format.

- DCF 77E (long wave reception only in Europe)
- 470 GPS 001 (Global satellite receiver)

The ERT internal software clock can alternatively be created by the application program, or be free running.

Validity reserve

A validity reserve can determine how long the module clock can continue running without external synchronization. The ERT data evaluated can be buffered with a maximum current consumption of 0.07 mA by the 140 XCP 900 00 battery module in the event of power loss. The current internal software time is transferred to the PLC at proportional intervals and enables the CPU clock to be set by the application program. For further information see *Time Synchronization with Standard Time, p. 23*.

User Functions and Services

2

Introduction

Overview

the 32 inputs of the 140 ERT 854 10 module can be individually preprocessed and transferred to the PLC as binary value, counter value or event. The following chapter describes the functions and services available.

What's in this Chapter?

This chapter contains the following topics:

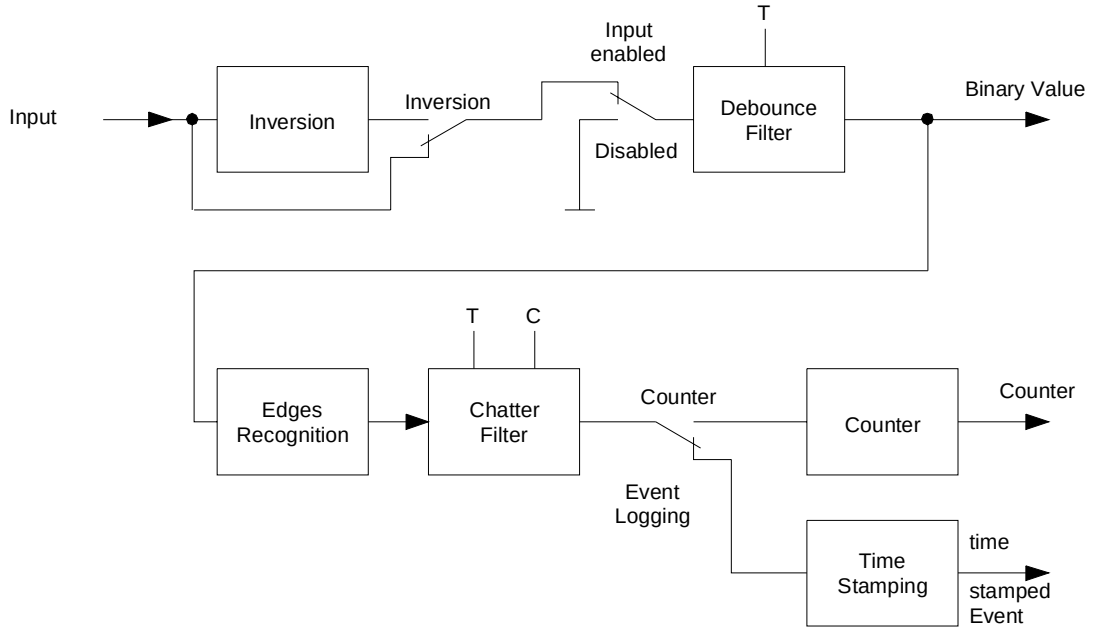
Input Processing - Registration and Filtering

Overview

The input signals connected to the 140 ERT 854 10 go through a multistage preprocessing stage before they are made available to the user program as binary, counter values or events. The preprocessing can be set with parameters for each individual input.

Signal Processing Sequence

The processing of the input signals is carried out according to the parameters set. Parametering is carried out via a Parameter configuration window (See *The Parameter Configuration Window, p. 51*).



Registration

Overview	The processing of the individual inputs is completely configurable: (disabled, inverted and with debounce time). The event inputs can also have a configurable chatter filter activated and an edge event evaluation.
Disabling	A disabled input always shows the value "0" independent for its input state
Inverting	The input polarity is inverted before further processing. If this is active, the opposite to the input signal status shown on the status LEDS is passed on for further processing.
Edge Recognition	Selects the edge transitions which should be used for active events and counter inputs. "Both Edges" processes rising and falling edges. Otherwise only a signal edge is processed: rising/falling, either with or without active inversion.

Filtering

Overview

The configurable filtering is done in 2 stages: debounce and dechattering.

CAUTION

Danger of incorrect interpretation of the input data

Filters are used to suppress the input recognition in a defined way. Filtering should only be used in a suitable way to prevent too much or undesired suppression of input data.

Failure to follow this precaution can result in injury or equipment damage.

Debounce

Debouncing can be used on all input functions and prevents the processing of fast state changes of the inputs, like for example, those caused by contact bouncing. Signal changes are ignored depending on the filter type and the preset time. The value range for the filter time is 0 to 255 ms; the value 0 deactivates the debounce filter. The selection of the debounce filter type "stable signal" or "integrating" affects all 8 function block inputs.

- "Stable Signal" Filtering: A signal change is only registered if the polarity change stays stable for longer than the filter time (each new change resets the filter time).
- "Integrating" Filtering: A signal change is only registered if the time integral of the input signal reaches the programmed filter time taking any polarity change into account.

Note: Debounce time>=1 ms is recommended to ensure enough immunity against electromagnetic disturbances. This means that input signal states >= 2 ms and events up to 250 Hz can be processed. In non-critical electromagnetic environments, the debounce time can be set to 0 to avoid unnecessary filter delays. This means that input signal states >= 1 ms and events up to 500 Hz can be processed.

Dechattering

Dechattering can only be used for event and counter inputs. It limits the number of events to a configurable value during a configurable time period. This should prevent multiple event registrations for the same input, e.g. disturbance influences due to slowly changing inputs (because the hysteresis is possibly set too small). The chatter counter is configurable for each individual input, the chatter time for each input pair. The selection of "dechattering" on the parameter screen activates the chatter filter for all 8 function block inputs. The chatter filtering for individual inputs can always be disabled by selecting the value of 0 as chatter count value. A "Chatter Filter Active" bit within the "status" output word (Bit 7 - DC) which is returned from the transfer EFB "ERT_854_10" (see *ERT_854_10: Data transfer EFB, p. 78*) signals that at least one "Chatter" input is being filtered. The bit is reset as soon as the chatter time of the last active filtered input has run out.

- Chatter time: The time period in which the chatter count limit has an effect. Value range from 1 ... 255 * 100 milliseconds = 0.1 ... 25.5 seconds.
- Chatter count: The maximum number of registered events which are allowed to be passed on within the chatter time period. Value range from 1 ... 255, the value 0 deactivates the chatter filter.

CAUTION

Danger of incorrect interpretation of the input data

Dechattering is a very powerful processing tool which can have undesired side effects. Its use with counter inputs is questionable. If edge recognition is performed for "both edges" then, in the case of odd-numbered chatter suppression, two successive events with the same edge (2 rising, 2 falling) appear when transferred to the PLC.

Failure to follow this precaution can result in injury or equipment damage.

Input Data Processing

Overview

The input signal can be used as binary inputs, counter values or for event recording depending on the parameters set in the Parameter configuration window (See *The Parameter Configuration Window, p. 51*).
Normally the input data of the ERT 854 module is processed by the corresponding EFBs (see *EFBs for the140 ERT 854 10, p. 71*)

Binary Inputs

All inputs of the function block are transferred to the PLC after the third processing stage (i.e. enabling, inverting and debounce filtering) before the chatter filter and edge recognition are performed. The processed values of all 32 inputs are cyclically transferred (every second PLC cycle) to the first and second input register word of the 7 word %IW register block of the ERT The address sequence of the module inputs corresponds to standard digital input modules, i.e. inputs 1 ... 16 correspond to bits 15 0. User confirmation is not necessary because the EFB ERT_854_10 must exist and be enabled. The processed values are available for all 32 inputs independent of their further processing as counter or event inputs. The input processing is always executed according to the configuration, but the ERT copies the processed values from the input immediately after the third input processing stage !

Note: If the BoolArr32 output array "Input" of the "ERT_854_10"-Transfer EFB (see *ERT_854_10: Data transfer EFB, p. 78*) is configured, the processed values are directly available as Bool values.

Counter Values

All inputs of the function block go through all five input processing stages (i.e. locking, inverting, debounce and chatter filtering as well as edge recognition). The count operation executes once edge recognition has been performed successfully. For edge recognition which is not set as "both edges", the configured inverting decides if rising or falling edges are counted.

Note: It is probably not worthwhile using inversion for the recognition of "both edges"

Counter values are 32 bit totals. The PLC receives a complete sequence (configured as: 8, 16, 24 of 32) of time consistent counter values in a multiplex procedure from the "ERT_854_10" transfer EFB cyclically (see description of the EFB, section *EFBs for the140 ERT 854 10, p. 71*). The EFB sets the values in the configured UDINTArr32 output array "Cnt_Data", without the confirmation of the user. After the transfer of the new counter values is completed, the EFB sets the signal "New Data", a Boolean variable "ND_Count", for one PLC cycle.

Note: The transfer of the counter values starts with function block 1 and ends with the last function block which is configured as counter inputs. If a consecutive sequence of function blocks starting with the first block are configured as counter inputs, transfer resources are saved. Since the transfer of the counter values competes with the transfer of the recorded events, faster reaction times for both types can be achieved if an ERT module is fully configured as either a counter or an event input. Binary and status inputs have no effect on this.

Event Logging

This function allows input state changes to be registered in time order with a high resolution. The input state changes are logged with a time stamp with high resolution. The events can later be shown in the correct sequence. The time stamping of events can be configured so that a group of 1, 2 or 8 inputs can be processed in parallel. All inputs of the function block go through all five input processing stages (i.e. locking, inverting, debounce and chatter filtering as well as edge recognition). The logging (including time stamping) is done as soon as the edge reaches the edge recognition. For edge recognition which is not set as "both edges", the configured inverting decides if rising or falling edges are logged.

Note: Inversion is probably not sensible to use with the recognition of "both edges".

A group of inputs is logged as an event if at least one of the inputs in this group has an edge which has been recognized, i.e.:

- any single input (1, 2 ... 7, 8),
- any input of an input pair (1-2, 3-4, 5-6, 7-8),
- an input of an 8 bit group.

Events contain a lot of information in an 8 byte block, including the processed values of all inputs in the group with the corresponding time stamp:

- Module number
- Type of input group and number of the first bit
- The current value of the inputs in the group
- Time stamp: Milliseconds
- Time stamp: Minute
- Time stamp: Hour
- Time stamp: Day of the week / Day in the month

The actual value of the inputs is stored right justified in an event structure byte. The ERT saves up to 4096 events in its battery backed FIFO buffer. The ERT provides error bits (bit 5/6 - PF/PH) for buffer overflow/buffer half full within the "Status" output word which is returned from the "ERT_854_10" transfer EFB. Individual events are transferred in a "ERT_10_TTag" structure to the PLC by the "ERT_854_10" transfer EFB. After processing the events, the user must actively signal readiness for the receiving of new events. See EFB description *ERT_854_10: Data transfer EFB, p. 78*. If desired, the parameter "Complete time report" can be selected to provide the month and year. For this purpose, there is a special pseudo event without values which contains the complete time information with month and year. The event is marked as a "Complete time report" and precedes the "actual", time stamped event. (See additional information about "Complete Time Report" in *Parameters and Default Values, p. 52*).

Status Inputs

Status word

The "Status" output word which is cyclically returned by the "ERT_854_10" transfer EFB contains the following error bits:

- D8 ... D0 ERT error bits
- D11 ... D9 reserved
- D15 ... D12 EFB error bits

A complete description of the error bits is in the *Division of the Error Bits, p. 88*
After the transfer of the new status inputs is completed, the EFB sets the signal "New Data", a Boolean variable from "ND_Stat", for one cycle.

Note: ERT/EFB error messages are displayed in the Unity Pro screen **Tools** → **Diagnostic Viewer** with the error number and explanation (see *Online error display, p. 90*).

Time Synchronization

3

Time Synchronization with Standard Time

Overview

The time stamped event logging requires a precise internal clock. The ERT module uses a software clock for creating the time in millisecond intervals. This software clock is normally synchronized with the help of an external time signal (standard time receiver) in one minute intervals. It can also be synchronized via a telegram or be free running.
The incoming time signal is checked for plausibility. Runtime deviations from the software clock are corrected. The time reception takes a few minutes before the time becomes available after startup. The software clock is synchronized to this time. The module then determines the deviation from the software clock with regard to the external clock within a specific period, and offsets the deviation accordingly. This is carried out continuously during the entire runtime. After a few hours runtime (generally within 2 hours) the software clock reaches maximum precision.
If implausible or incorrect time messages are received, the software clock continues running without synchronization. The deviation gets larger during this time. If this time phase does not exceed the "Validity Reserve" specified, the clock resynchronizes when the next valid time information is received. However, if the time period is exceeded before the module receives a valid time signal, the ERT sets bit "Time Invalid" in the "Status" output word (bit 3 - TU), returned by the "ERT_854_10" transfer EFB (see *ERT_854_10: Data transfer EFB, p. 78*). All time stamps set after this are invalid (the high priority byte for millisecond information is set to FF). The bit is reset as soon as the next valid time message is received.
If the module receives no valid time messages for 10 minutes, the ERT sets the bit "Time Reference Error" in the "Status" output word (bit 2 - TE), returned by the "ERT_854_10" transfer EFB (see *ERT_854_10: Data transfer EFB, p. 78*). The bit is reset as soon as the next valid time message is received.

Synchronization

There are three types of synchronization available:

- DCF 77E reception module (German standard - long wave reception only in Europe)
- 470 GPS 001 00 satellite receiver, DCF77 formatted signal given (global satellite reception)
- Synchronized by the PLC using "ERT_854_10" EFB (low precision)

DCF Time base

The DCF 77E receiver delivers a 24VDC signal in DCF77 format and can supply up to 16 ERT modules concurrently. The BCD coded time signal is transferred once a minute and synchronizes the ERT minutes changeover. When the ERT is restarted the software clock is synchronized within three minutes of receiving the first information. After this the ERT software clock time matches the standard time sender. If the send signal becomes unavailable the free running software clock can still be used but is not as precise. The DCF sender delivers CET (Central European Time), takes into account summer/winter time changes as well as seconds and years transitions.

GPS Time base

A GPS receiver such as the 470 GPS 001 must be used for applications which use GPS satellite time references. This module demodulates the GPS signal and delivers DCF77 format output signal from 24 VDC. The ERT decodes the signal and synchronizes the minutes transition for the internal software clock. GPS satellites sends UTC time (Universal Time Coordinated) which GMT (Greenwich Mean Time = Western European Time) corresponds to. Seconds and years transitions are taken into account. Depending on the location, the local time relative to GMT as well the local summer/winter time changes can be configured with the 470 GPS 001 receiver. The recommended validity reserve for the DCF/GPS time base signal is one hour (the settings range for DCF/GPS sync is between 1 ... and 5 hours). Several ERT module groups can be synchronized simultaneously using a GPS receiver. Further information can be found in the manual for 470 GPS 001 00 Receivers.

EFB synchronized internal clock

If a clock only requires a lower precision, the ERT internal software clock can be synchronized with a time value sent by the master. The software clock runs freely until the next time value is received. Precision is usually within 100 milliseconds per hour and the software clock must be synchronized correspondingly often. The "ERT_854_10" transfer EFB provides the required time synchronization. This means several ERT modules can be supplied with almost the same time; the time source used is the derived data structure "DPM_Time". The validity reserve setting for the EFB synchronized internal software clock moves within the area 1 ... and 254 hours). However, if the time period is exceeded before the next transfer of a time signal, the ERT sets bit "Time Invalid" in the "Status" output word (bit 3 - TU), returned by the "ERT_854_10" transfer EFB. All time stamps set after this are invalid (the high priority byte for millisecond information is set to FF). The bit is reset as soon as the next valid time message is received.

Free running internal clock

The ERT internal software clock can also be used on its own. Setting the validity reserve for the internal software clock to 0 activates duration mode, shown by the bit "Time not synchronized" in the "Status" output word (bit 4 - TA) which is returned by the "ERT_854_10" transfer EFB. In this case there is no validity reserve that can be exceeded and therefore no invalid time stamps. The bits "External Reference Error" and "Time Invalid" in the output word "Status" (Bit 2/3 - TE/TU) are never set; the time starts automatically without synchronization. The default start settings for the internal clock is 0 hours, 1/1/1990. The time settings can be made using:

- a telegram (e.g. by IEC 870-5-101)
- the CPU clock (using the "DPM_Time" data structure)

.

Note: Using the free running internal software clock enables even more precise processing of events within an individual ERT.

Typical Application Areas

4

Typical areas of application

Overview

The ERT 854 10 is particularly suited for determining the binary input status and counter value that require a time stamp

140 ERT 854 10 Applications

The following areas of application are valid for the 140 ERT 854 10:

- Processing binary inputs: Use as a standard I/O module with filtering and an input range of 24 - 125 VDC.
- Event Logging: The event of an individual process status can be logged with the corresponding time (time stamp). This enables the later reconstruction of the time point and the sequence of process signals "coming" or "going".
- Counter value: Use as a standard I/O module (with filtering, 32 bit summing with max. 500 Hz) with an input range of 24 - 125 VDC.
- Periodic time stamping of process values: Recording counter values in defined time intervals. The combined use of both function groups can be used as an advantage here.
- Time dependent switching actions: Outputs can be set regardless of time for contolling lighting, heating, ventilators, temperatures (building automation), or for opening/closing doors, machines, ... (safety measures). The output status can be recorded with the ERT.

Module Description

II

Introduction

Overview

The 140 ERT 854 10 is an intelligent digital input module for evaluating input values with or without event recording.

What's in this Part?

This part contains the following chapters:

Module Description

5

Introduction

Overview

This chapter provides information about the structure of the 140 ERT 854 10 module and its technical data.

What's in this Chapter?

This chapter contains the following topics:

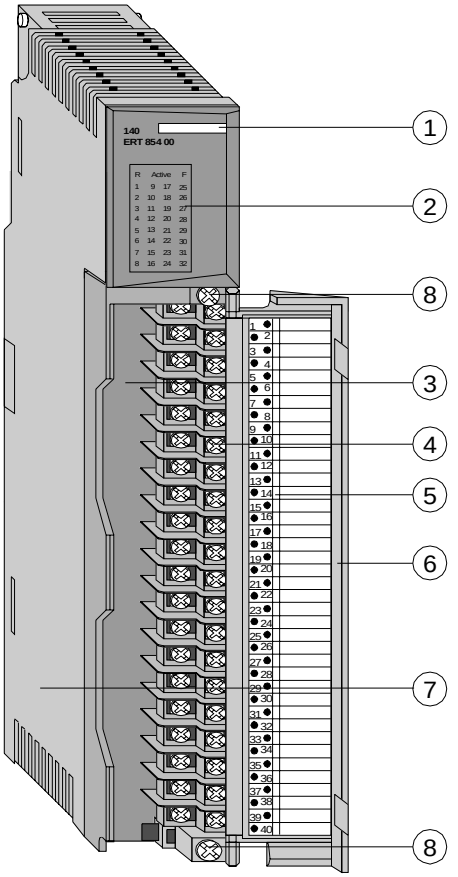
Overview

Introduction

The 140 ERT 854 10 is a Quantum Expert Module with 32 binary inputs (24 ... 125 VDC). The module is suitable for the evaluation of digital inputs, counter pulses and events.

Front View of the Module

Front View of the ERT 854 10



Location of Operating Elements

1 Color Code

2 Display field (LEDs)

3 Terminal Block

4 Connection terminals

5 Sliding Label (inside)

6 Cover for the terminal blocks

7 Standard housing

8 Screws for terminal block

Features and Functions

Features

The ERT 854 10 is a Quantum Expert Module with 2 groups of 16 binary inputs (24 ... .125 VDC). The input groups are potentially isolated to each other and to the internal logic. In addition to the counter pulses, digital input values with our without even

Mode of Functioning

The registers of the ERT 854 10 count impulses with frequencies of up to 500 Hz with an interruption/impulse period of 1 ms and provide these values as 32 bit counter values for the CPU. The module is logically divided into 4 blocks of 8 inputs. The inputs of each block can be processed as binary input signals, event or counters, depending on the parameters set.
The input processing (debounce time, edge recognition and inversion) can be configured separately for each input.
The module supports DCF77 formatted time receivers over a 24 VDC input.

Planning

What is to be planned

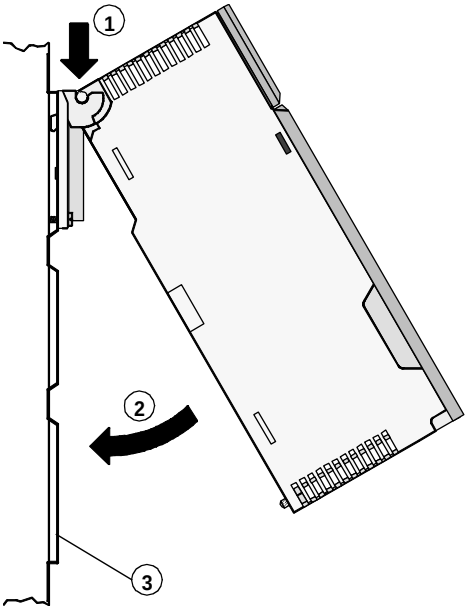
You plan:

- a slot in the Quantum rack (local or RIO station).
- the ERT Paramteres. Each of the 4 ERT 854 10 input blocks can be configured with a different functionality (e.g. counters or inputs with our without event recording).
- the connection of the reference voltage for each input group.
- the Process Peripherials Connection.
- the connection of an external time receiver.

Mounting Position in the Rack

Insert the module in any I/O slot on the Quantum and screw it to the rack. The module must be screwed into position to ensure correct operation (EMC).

Mounting the Module



1 Insert the module

2 Screw the module to the rack

3 Rack

Module Cabling

Overview

This section describes the connection of time receivers, supply voltages and external input signals.

Reference Voltage

The input voltage range for the inputs is defined with the reference voltage. Reference voltages and input signals of the same group are to be protected with a common fuse. In addition, the inputs can also be individually protected.

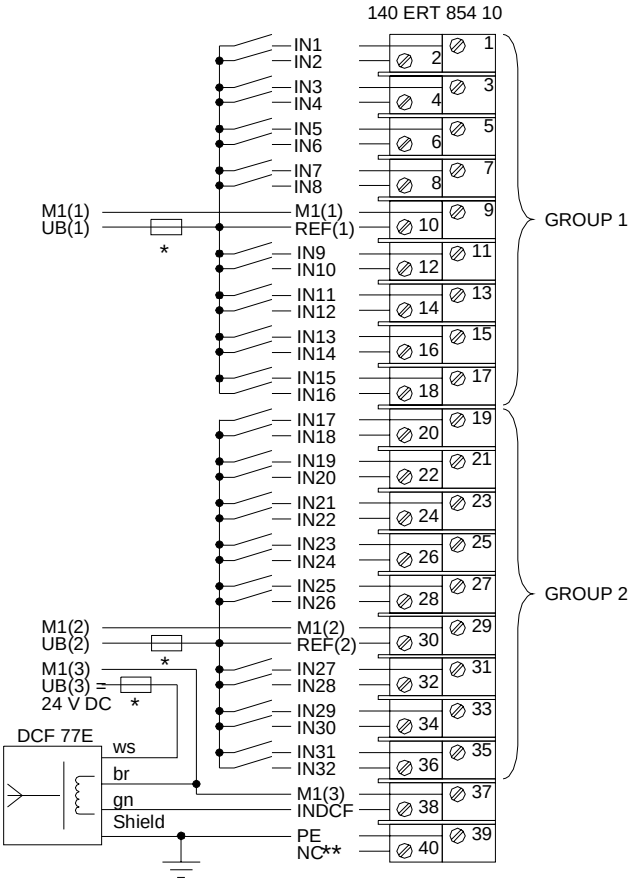
CAUTION

Damage of the Module

Never use the ERT module without a proper reference voltage to avoid damage to the module.

Failure to follow this precaution can result in injury or equipment damage.

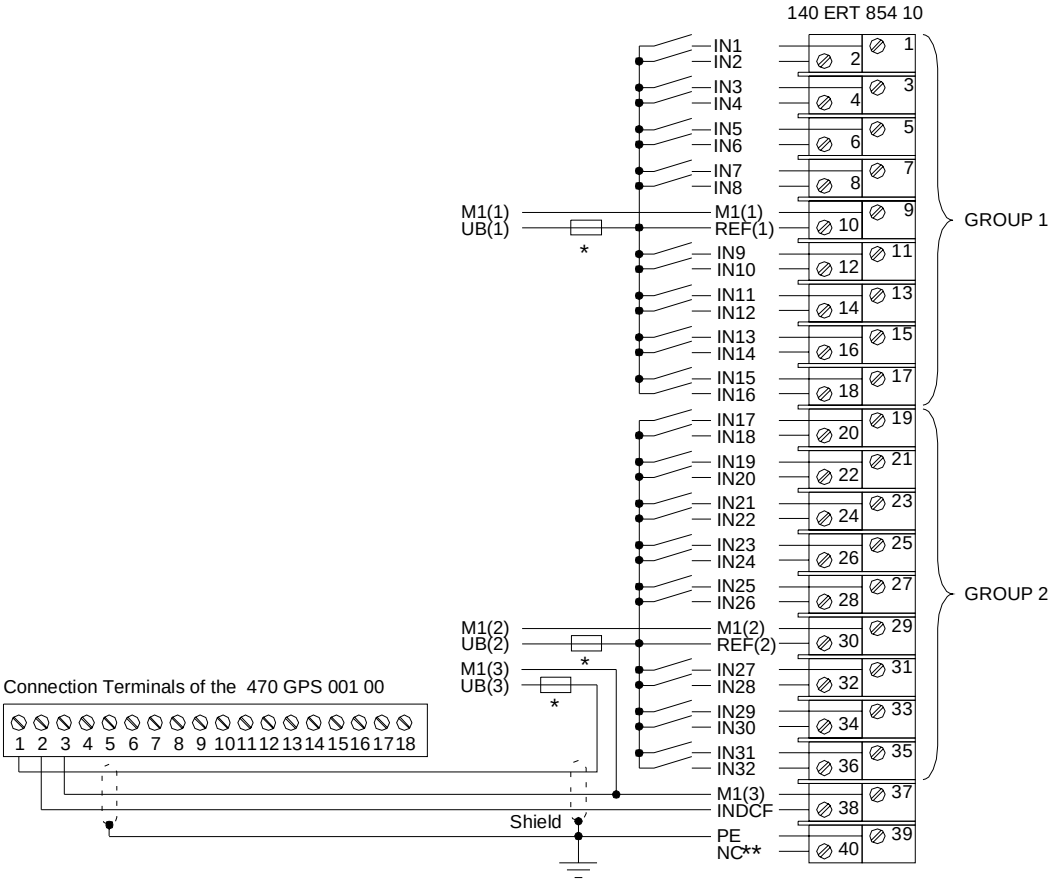
DCF 77E Connection example for the ERT 854 10 with a DCF 77E time receiver



***** UB(1), UB(2):24 ... 125 VDC, UB(3): 24 VDC, separate protection recommended

****** not connected, suitable for support clamp for UB(3)

GPS 001 Connection example for the ERT 854 10 with a GPS 001 time receiver



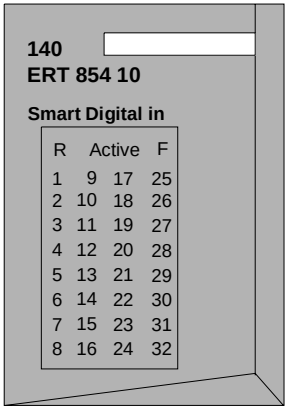
***** UB(1), UB(2):24 ... 125 VDC, UB(3): 24 VDC, separate protection recommended

****** not connected, suitable for support clamp for UB(3)

Diagnosis

Condition Display

The modules have the following indicators:



Meaning of the Indicators:

Indicators:	Color	Meaning
R	green	ready. Self test successful when voltage connected The firmware is running correctly and the module is ready for operations.
Active	green	The communication with the Quantum CPU is active.
F	red	Group Error. Lights when the configured error occurs.
1 ... 32	green	Input Signal. Indicator for process input signal "1".

Technical data

Supply

Data of the Supply

Reference voltage for each process input group	24 ... 125 VDC, (max. 18 ... 156 VDC)Current consumption per group: max. 3 mA
internal via the rack	5 VDC, max. 300 mA
Current requirements for buffer operation	maximum 0.07 mA from XCP 900 00

Process Inputs

Data of the Process Inputs

Number	32 in 2 Groups			
Input Voltage	24 ... 125 VDC			
Potential isolation	Inputs to the Quantum Bus, Group 1 to Group 2 (Opto-coupler)			
Debounce time	0 ... 255 Millisecunds (configurable)			
Inversion	Set with parameters			
Max. Cable length	400 m unshielded, 600m shielded			
Switching Level: Nominal voltage for the input signals Min current for a 1 signal	 24V 6mA	 48V 2.5mA	 60V 2.5mA	 125V 1mA
Signal level 0 signal Signal level 1 signal	nominal 0% of the group reference voltage, max. +15 %, min. -5 % nominal 100% of the group reference voltage, max. 125 %, min. 75 %			
Internal power loss from all process inputs	max 7.5 W			

Input for the time receiver

Data for the time receiver

Number	1, DCF77 Data format from DCF- 077E or GPS - 470 001 00
Input Voltage	24 VDC
Potential isolation	Optocoupler
Time Stamp resolution	1 ms
Current consumption	5 mA

Mechanical structure

Dimensions and Weight

Format	Width = 40.34 mm (Standard Housing)
Mass (weight)	0.45 kg

Connection Type

Data of the Connections

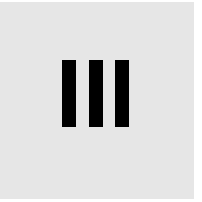
Process Inputs, DCF receiver	40 pins Terminal Block

Environmental conditions

Data of the Environmental Conditions

System Data	See Quantum User Manual
Power loss	Max. 9W, typical 5W

Configuration



Introduction

Overview

The 140 ERT 854 10 in included in Unity Pro as a standard module. This section describes the configuration of the modules and the parameterization of the corresponding EFBs. An example is given for the most important applications.

What's in this Part?

This part contains the following chapters:

Quantum Addressing Modes

6

Overview

Purpose

In the functional description of this Expert Module the register addressing (3x, 4x) established in the Quantum world is widely used. To allow the user an easy transition to the addressing modes provided by Unity Pro, this chapter describes the different modes Unity Pro allows to address the data from a Quantum module:

- Flat Addressing
- Topological Addressing

What's in this Chapter?

This chapter contains the following topics:

Flat Addressing

Flat Addressing

The Quantum modules follow a flat address mapping. Each module requires a determinate number of bits and/or words to work properly. This addressing mode is equivalent to the former used register addressing with the following assignments:

- 0x is now %M
- 1x is now %I
- 3x is now %IW
- 4x is now %MW

To access the I/O data of a module the address range entered in the configuration screen for the module is used.

Examples

The following examples show the relation between the register addressing and the IEC addressing used in Unity:

000001 is now %M1
100101 is now %I101
301024 is now %IW1024
400010 is now %MW10

Topological Addressing

Topological Addressing

The topological addressing allows to access I/O data items using the topological location of the module within a system.
The following notation is used:

```
%<Exchangetype><Objecttype>[\b.e\]r.m.c[.rank]
```

Used abbreviations: **b** = bus, **e** = equipment (drop), **r** = rack, **m** = module slot, **c** = channel

Note: The [\b.e\] defaults to \1.1\ in a local rack and does not need to be specified. The rank is an index used to identify different properties of an object with the same data type (e.g. value, warning level, error level). The rank numbering is zero-based and the rank can be ommited in case of being zero.

For detailed information on I/O variables, please refer to Direct addressing data instances in the *Unity Pro Reference Manual*.

Example

To read the input value (rank = 0) from channel 7 of an analog module located in slot 6 of a local rack:

```
%IW1.6.7[.0]
```

For the same module located in drop 3 of a RIO bus 2:

```
%IW\2.3\1.6.7[.0]
```

To read the 'out of range' (rank = 1) from channel 7 of an analog module located in slot 6 of a local rack:

```
%I1.6.7.1[.0]
```

Addressing Example

Example for the 3 Addressing Modes

The following example compares the 3 possible addressing modes. An 8-channel thermocouple 140 ATI 030 00 module with the following configuration data is used:

- mounted in slot 5 of the CPU rack (local rack)
- starting input address is 201 (input word %IW201)
- end input address is 210 (input word %IW210)

To access the I/O data from the module you can use the following syntax:

Module data	Flat addressing	Topological addressing	IODDT addressing	Concept addressing
Channel 3 temperature	%IW203	%IW1.5.3	My_Temp.VALUE	300203
Channel 3 out of range	%IW209.5	%I1.5.3.1	My_Temp.ERROR	300209 Bit 5 to be extracted by user-logic
Channel 3 range warning	%IW209.13	%I1.5.3.2	My_Temp.WARNING	300209 Bit 13 to be extracted by user-logic
Module internal temperature	%IW210	%IW1.5.10	not accessible through IODDT	300210

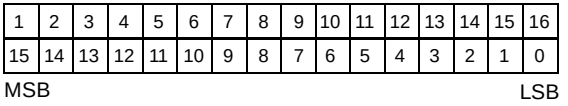
Note: For the IODDT the data type `T_ANA_IN_VWE` is used and the variable `My_Temp` with the address `%CH1.5.10` was defined.

For comparison, the register addressing as used with Concept is added in the last column. As Concept does not support direct addressing of a bit in a word, the bit extraction has to be performed in the user program.

Discrete I/O Bit Numbering

Introduction

The numbering of channels of an I/O module usually starts with 1 and counts up to the maximum number of supported channels. The software however starts numbering with a 0 for the least significant bit in a word (LSB). Additional the Quantum I/O modules have their lowest channel mapped to the most significant bit (MSB). The following figure shows the mapping of I/O channels related to the bits in a word:.



Word Addressing versus Bit Addressing

Mainly discrete I/O modules can be configured to deliver their I/O data either in word format or in bit format. This can be selected during configuration by selecting either %IW (%MW) or %I (%M). If you need to access a single bit from an I/O module configured to use an I/O word, you can use the syntax %word.bit. The following table gives you the connection between I/O point number and the belonging I/O address in bit and word addressing.
The table shows an 32-point input module in the main rack, slot 4 configured with starting address %I1 or %IW1:

I/O channel	Bit address (flat addressing)	Bit address (topological addressing)	Bit address extracted from word (flat addressing)	Bit address extracted from word (topological addressing)
1	%I1	%I1.4.1[.0]	%IW1.15	%IW1.4.1.1.15
2	%I2	%I1.4.2[.0]	%IW1.14	%IW1.4.1.1.14
3	%I3	%I1.4.3[.0]	%IW1.13	%IW1.4.1.1.13
		• • •		
15	%I15	%I1.4.15[.0]	%IW1.1	%IW1.4.1.1.1
16	%I16	%I1.4.16[.0]	%IW1.0	%IW1.4.1.1.0
17	%I17	%I1.4.17[.0]	%IW2.15	%IW1.4.1.2.15
18	%I18	%I1.4.18[.0]	%IW2.14	%IW1.4.1.2.14
		• • •		
31	%I31	%I1.4.31[.0]	%IW2.1	%IW1.4.1.2.1
32	%I32	%I1.4.32[.0]	%IW2.0	%IW1.4.1.2.0

Addressing

Flat Addressing

This module requires 7 contiguous, 16-bit input words (%IW), and 5 contiguous, 16-bit output words (%QW).

Topological Addressing

Topological addresses for the 140ERT85410 Time Stamp Module:

Point	I/O Object	Comment
Input 1	%IW[\b.e\]r.m.1.1	Data
	• • •	
Input 7	%IW[\b.e\]r.m.1.7	Data
Output 1	%QW[\b.e\]r.m.1.1	Data
	• • •	
Output 5	%QW[\b.e\]r.m.1.5	Data

Used abbreviations: **b** = bus, **e** = equipment (drop), **r** = rack, **m** = module slot.

Note

The above described addressing is for information only. Direct access to the modules raw data is not recomended. All data exchange should be performed through the EFBs for the ERT module.

The Parameter Configuration Window

7

The Parameter Configuration Window

Call

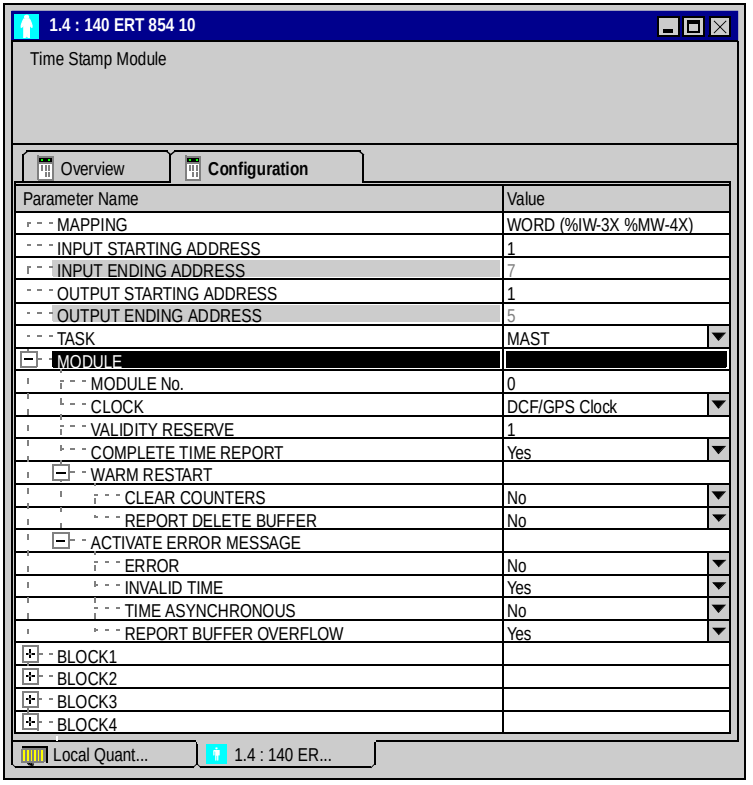
You can access the Parameter Configuration window for the 140 ERT 854 10 module by double-clicking on a module in the Quantum rack.
You can also open the configuration window by clicking on the module with the right mouse button.

Structure of the Parameter Configuration Window

The Parameter Configuration window contains general parameters for the module and the specific parameters for the four function blocks.
The parameters have been preset to default values contained in the "I/O Image", and can be modified by the user.
Parameters can only be edited when the application program is not running.

Parameters and Default Values

Structure of the Parameter Configuration window, general parameter

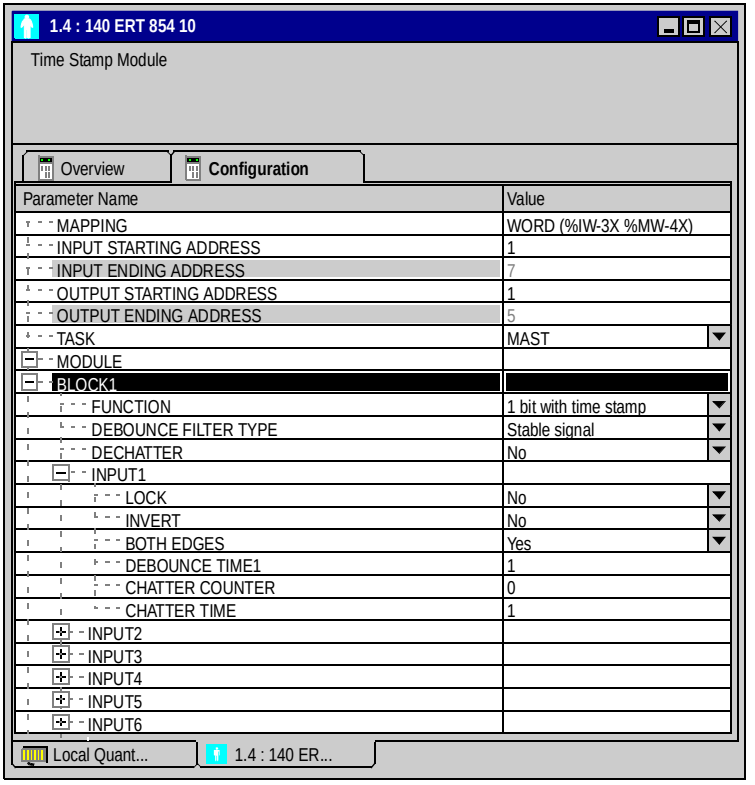


The following table provides an overview of the general module parameters and their default values.

Name	Default value	Options	Meaning
Mapping	WORD (%IW-3X %MW-4X)	-	The default value cannot be changed because the ERT 854 10 module normally reads the raw values from the input words (%IW-3X) and writes them to the output words (%MW-4X).
Input starting address	1	-	Input starting address
Input ending address	7	-	The ending address for the inputs results from the starting address for the inputs plus 6 because the module occupies seven %IW registers.
Output starting address	1	-	Output starting address
Output ending address	5	-	The ending address for the outputs results from the starting address for the inputs plus 4 because the module occupies five %MW registers.
Task	MAST	MAST/FAST/ (AUX0/AUX1/ AUX2/AUX3 only with CPU 651 50)	MAST = Master Task is assigned FAST = Fast Task is assigned AUX = AUX Task is assigned The settings for MAST/ TASK/ AUX are defined during CPU configuration.
MODULE:			
Module No.	0	1... 127	User defined, inserted in event message. The uniqueness of the value is not checked. 0 = Default, no selection made
Clock	DCF/GPS Clock	DCF/GPS Clock	External synchronization in DCF77 format by the DCF or GPS clock.
		Internal clock	Telegram synchronization. The clock runs either without monitoring or is monitored within a validity reserve.
		No	Internal clock is deactivated
Validity reserve	1 hour	1 ... 254 hours	Internal clock: Time from the last synchronization until setting the TU bits and the time until the time stamp becomes invalid.
		0	Internal clock: 0 = free run mode without elapsed time (TE/TU bits are not set)
		1 ... 5 hours	DCF/GPS Clock: 1 hour recommended

Name	Default value	Options	Meaning
Complete time: Output	Yes	No/yes	Switches the transfer of the complete time telegram (with month and year) on or off. Transfer of the complete time report is made as dummy event 1x directly before a time stamp event: the prerequisite is ALWAYS transferring a time stamp event for monthly transitions, every start/stop of user programs, clearing the time stamp buffer, starting/setting the clock, otherwise the complete time report telegram is not sent.
Warm restart:			
Clear counters	No	No/yes	Clear counter on warm restart
Clear message buffer	No	No/yes	Clear FIFO buffer on warm restart
Activate Error Messages			
DCF/GPS Error	No	No/yes	Error values shown by the error LED "F". The enabled bits are treated as errors. Every disabled bit is treated as a warning (the error bits for an error during a self test are always set).
Invalid time:	Yes	No/yes	
Time Asynchronous	No	No/yes	
Message Buffer Overrun	Yes	No/yes	

Structure of the Parameter Configuration window, specific parameters for the four function blocks



The following table provides an overview of the specific parameters for the four function blocks and their default values. The parameters can be set individually for each block.

Name	**Default value**	**Options**	**Meaning**
BLOCK1	1 - 4	1 - 4	Number of the selected function block.
Function	1 bit with time stamp	Binary	Only binary inputs
		Counter	Binary and counter values
		1 bit with time stamp	Binary + 1 bit event logging
		2 bit with time stamp	Binary + 2 bit event logging
		8 bit with time stamp	Binary + 8 bit event logging
Debounce filter	Stable signal	Stable signal/ integrated	Debounce filter mode
Dechatter	No	No/yes	Disabling/enabling the chatter filter

The following parameters refer to all individual inputs (**Exception:**Chatter time refers to two inputs next to each other)

Name	Default value	Options	Meaning
INPUT1	1 - 32	1 - 8, 9 - 16, 17 - 24, 25 - 32	Input number sequence for the function block selected
Disabled	No	No/yes	Impedes processing of input data for the input (always 0)
Inverted	No	No/yes	Reverse polarity of the input
2 Edges	Yes	No/yes	Edge monitoring for both edges
Debounce time	1	0 .. 255	Debounce time 0 ... 255 milliseconds 0 = without internal SW delay
Chatter number	0	0 .. 255	Chatter number 0 ... 255 (for event/counter inputs) 0 = Chatter filter deactivated
Chatter time	1	1 .. 255	Chatter filter time duration 1 ... 255*0.1 seconds **Note:** This setting refers to two inputs next to each other!

Startup the140 ERT 854 10

8

Introduction

Overview

This chapter describes the preconditions and boundary conditions required for starting the 140 ERT 854 10 and provides a check list with the necessary steps.

What's in this Chapter?

This chapter contains the following topics:

140 ERT 854 10 Module and Resource Limitations

Limitations

Check whether the following conditions have been adhered to before starting the configuration:

- Unity Pro V 1.0 or higher
- Can be used in local or remote module racks (RIO) with RIO Drop Firmware higher than V1
- Cannot be used in DIO Drops
- Up to 9 ERTs can be mounted on each local or remote module rack (several module racks possible)
- Processing signal status > 1 millisecond + filter time possible
- Counter inputs up to 500Hz with 32 bit addition
- Each ERT requires an "ERT_854_10" transfer EFB
- 7 INPUT words, 5 OUTPUT words per ERT
- Several ERT modules can be connected to one standard time receiver. The 140 ERT 854 10 requires 5 mA from the receiver
- Maximum power consumption of 0.07mA from the battery module XCP 900 00 required for receiving counter, event FIFO buffer and parameter data.

Time receiver

The standard time receiver must provide an output signal in DCF77 format for 24 VDC.

The following standard time receivers are provided:

- DCF77E: DCF long wave receiver for Europe
- 470 GPS 001 00: A GPS satellite receiver

DCF Receiver

Overview

The DCF 77E module operates as an internal receiver with integrated antenne. The module receives and converts the received time signal in a 24 VDC signal in DCF77 format, and amplifies it before sending it on to the 140 ERT 854 10 module.

DCF Signal

The time signal received in the Central European Time zone is known as the DCF77 and provides CET. It is sent from the atomic clock to the National Institute for Science and Technology Braunschweig, Germany, and sends a long wave signal of 77.5 kHz (from which DCF77 derives its name) via a transmitter in Frankfurt am Main. The signal can be received throughout Europe (in a radius of approximately 1000 km from Frankfurt).
When selecting a location for erecting an antenne, the following sources of interference should be taken into account which could disturb or destroy signal reception through their DCF receivers:

- electromagnetically contaminated areas. Avoid areas with potential sources of interference, such as strong transmitters, switching stations and airports. Strong interference can also be caused industrial machinery and cranes.
- Steel supports in buildings, rooms and appartments. Poor reception can occir in cellars, underground car parks and closed operating cabinets.
- "Shadows" and "dead band" in mountain areas, high buildings, ...

The GPS Receiver

Overview

The 470 GPS 001 00 module is a GPS time signal receiver. Other usual GPS standard time receivers can also be used as long as they deliver the time signal in DCF77 format with a 24 VDC potential.

GPS Signal

A group of lower orbiting GPS satellites (Global Positioning System) send radio signals from which entensive time information can be derived. Their orbits are distributed evenly so that every point on earth is covered by at least 3 different satellites. The GPS signal can be received accross the whole world. The absolute time precision achieved by the GPS signal is considerably higher than that reached by the DCF receiver.

GPS satellites sends UTC time (Universal Time Coordinated) which corresponds to GMT (Greenwich Mean Time). Seconds and years transitions are taken into account. The 470 GPS 001 can be configured using a time offset from UTC corresponding to the local time zone. Summer/winter time change overs can be configured likewise.

Calendar and day data is diverted from the GPS signal and transferred to the 140 ERT 854 10 module.

The antenne must be ordered separately from the GPS receiver. More details are contained in the technical data section of your reciever.

When selecting a location for erecting an antenne, the following sources of interference should be taken into account which could disturb or destroy signal reception through their GPS receivers:

- electromagnetically contaminated areas: Avoid areas with potential sources of interference, such as strong transmitters, switching stations and airports.
- limitred to the sky and the horizon: The antenne must be erected outside to ensure disturbance operation. Enclosed spaces or operating cabinets impedes satellite reception.
- Length of the antenne cable: Do not exceed the maximum permitted length of the antenne cable
- Atmospheric conditions: Heavy snowfall and rain can impede your GPS receiver or even prevent any signal reception.

Behaviour when starting/restarting and the data storage

Cold Start

This is the default behavior of the ERT when connecting or reconnecting a stabile power supply.

- All recorded events, counter values and the current parameters of the ERT are initialized with a defined state.
- The recording of the process data is delayed until the PLC has been started and can therefore provide the ERT with a valid parameter set.
- Since the ERT does not have a hardware clock, the internal software clock is invalid until it has been synchronized in a suitable form:
  - Depending on the source which has been configured for time synchronization, the time stamps for all recorded events are set to invalid time until either: the internal clock is set with a DPM_Time value using the EFB or time synchronization with an external time signal has occurred.
  - A special case: If the "clock" parameter of the ERT was configured as an "internal clock" in free running mode (with a power reserve of zero), the internal clock starts with a default setting at hour 0 on 1/1/1990.
- If a "complete time report" has been configured, a complete time transfer is done directly before the first recorded event so that the clock synchronization follows.

Data Storage

The current data of the ERT 854 10 can be protected from a power loss if the rack has a 140 XCP 900 00 battery module. If the supply voltage falls below a defined limit, it will be recognized by the rack. All recorded data, counter values and the current parameter set are saved in a non-volatile RAM by the firmware and remain until the next warm start (see below). In situations where the saving in the ERT does not happen (5 VDC short circuit or hot swap of the ERT module), a cold start is performed.

Warm Start

Reconnecting a stabile supply voltage causes a warm start of the ERT module, as long as the module is in a state where it can store the current data in a consistent form.

- All recorded events, counter values and the current parameters of the ERT are restored from the non-volatile RAM.
- If the "warm start" parameters ("Clear counter"/"clear message buffer") are configured, the recorded events and/or counter values are erased.
- Recording of the process data with the ERT is immediately continued with the same parameter set even if the PLC is not started yet or the remote connection could not be restored at this time.
- Since the ERT does not have a hardware clock, the software clock is invalid until it has been synchronized in a suitable form:
  - Depending on the source which has been configured for time synchronization, the time stamps for all recorded events are set to invalid time until either: the internal clock is set with a DPM_Time value using the EFB or time synchronization with an external time signal has occurred.
  - A special case: If the "clock" parameter of the ERT was configured as an "internal clock" in free running mode (with a power reserve of zero), the internal clock starts with a default setting at hour 0 on 1/1/1990.
- If a "complete time report" has been configured, a complete time transfer is done directly before the first recorded event so that the clock synchronization follows.
- If the corresponding "ERT_854_10" transfer EFB is active in the PLC again, the transfer of the events and counter values in the FIFO buffer of the ERT is continued. Current binary input values and status words are also transferred.
- If the PLC provides a new parameter set when starting which would mean a change in the time of process data evaluation, all recorded events and counter values are cleared since they would no longer be consistent with the new parameter set.

Check List

Step by Step

The following steps are to be performed for successfully start-up of the 140 ERT 854 10:

Step	Action
1	Install the 140 ERT 854 10 module in the local or remote rack.
2	Connect the designated process peripherals and the standard time receiver to the module (see *Module Cabling, p. 36*).
3	Do not forget to connect the reference supply voltage for the ERT input groups. **Note:** Please ensure that the installation guidelines for the antennas for the standard time receiver are followed.
4	Enter the 140 ERT 854 10 in the I/O map. **Note:** Take special note that the module requires seven %IW registers and five %MW registers in state RAM.
5	Configure the 140 ERT 854 10 in the corresponding Parameter Configuration window to provide the required functionality (see *The Parameter Configuration Window, p. 51*.
6	Use the correct EFB from the I/O management function block library (Quantum I/O configuration family) to provide the "slot" input parameter for the "ERT_854_10" transfer EFB. either QUANTUM for local and DROP for remote module racks (see *DROP: Configuring an I/O station rack, p. 73* or *QUANTUM: Configuring a main rack, p. 76*).
7	Define EFB user data structures for the required data types. Events can be "used", for example, by outputting them to a printer or storing them in central data storage.
8	Use the "ERT_854_10" transfer EFB from the I/O management function block library (Expert I/O module family) to transfer ERT data (see *ERT_854_10: Data transfer EFB, p. 78*). **Note:** The transfer of new events with the "ERT_854_10" EFB overwrites the previous event information. Therefore the user confirmation should only be provided when the data has been completely evaluated and is no longer needed.
9	Please note the difference in the behavior of the ERT when starting/restarting depending on if the rack has an XCP module (see *Behaviour when starting/ restarting and the data storage, p. 61*).

Integration in the Application Program

9

Introduction

Overview

The chapter contains information about how the ERT 854 10 module and respective EFBs are inserted in the Unity Pro application program.

What's in this Chapter?

This chapter contains the following topics:

Integrating Intelligent I/O Modules

Introduction

EFBs are provided for integrating intelligent I/O modules. The EFBs are designed so that the program can be created as independently as possible from the hardware module used. The project specific information is processed and stored in data structures on the PLC using hardware dependent EFBs (e.g. ERT_854_10). The ERT_854_10 data transfer EFB works with these data structures. It reads the raw values from the Input words (%IWx), processes them and writes the ERT handshake and clock synchronization data to the output words (%MWx). The result of this is that changes of direct addresses or changes of the input or output parameters are automatically evaluated by the EFBs.

Dividing into sections

Since the evaluation of the configured data is only done once after loading, it is recommended that the EFBs for linking to intelligent modules are divided into several sections.
A division into at lease two sections is recommended.

- Configuration section
- Processing section

By division into a configuration section and several processing sections, the CPU load can be reduced because the configuration section only has to be executed once (after a restart or a warm start). The processing section must usually be executed continuously.
The configuration section is controlled with the EN inputs of the corresponding EFB. The EFBs are enabled with internal variables that are set to 1 in the first cycle.

Configuration Section

Configuration section

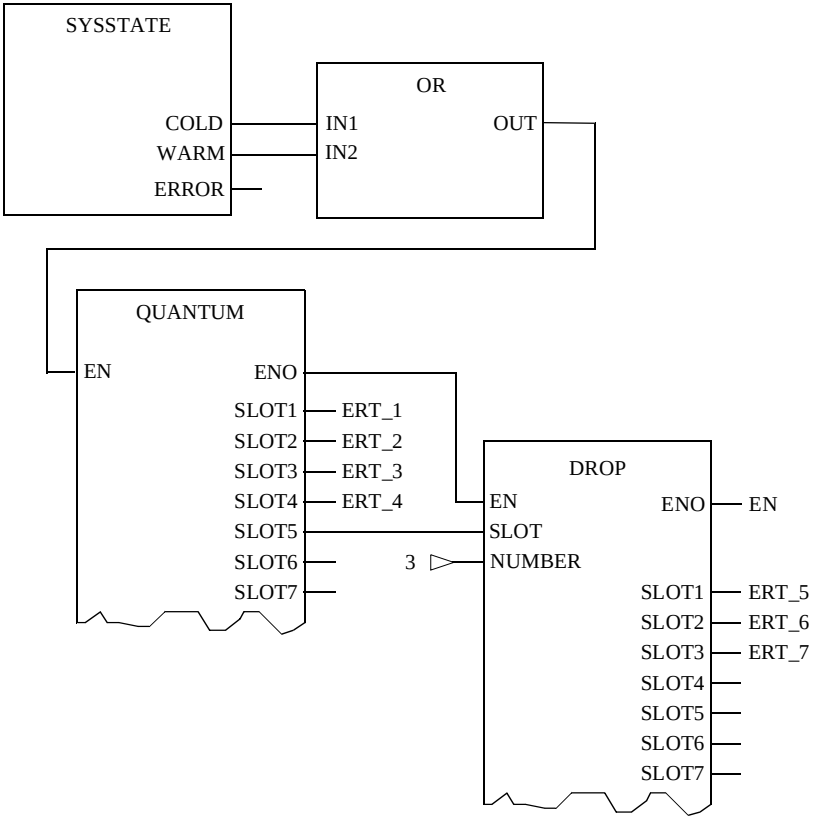
The configuration section is used to configure the analog input and output modules and controls data exchange between the analog EFBs, the State Ram and the configuration data.
The configuration section should be called `CfgErt` and the internal variable which controls it should be called `CfgErtDone` to guarantee the compatibility to future Unity Pro versions.

There are 2 possibilities for the control of the configuration sections:
- using the `EN` inputs of the individual EFBs
- enabling or disabling the configuration section.

Controlling the Configuration Section

Control of the configuration section is possible through the EN inputs of this section's individual EFBs. The EFBs are enabled through the SYSSTATE EFB which has COLD or WARM outputs that are set to 1 for one cycle after either a cold or a warmstart.

Example of a CfgErt configuration section



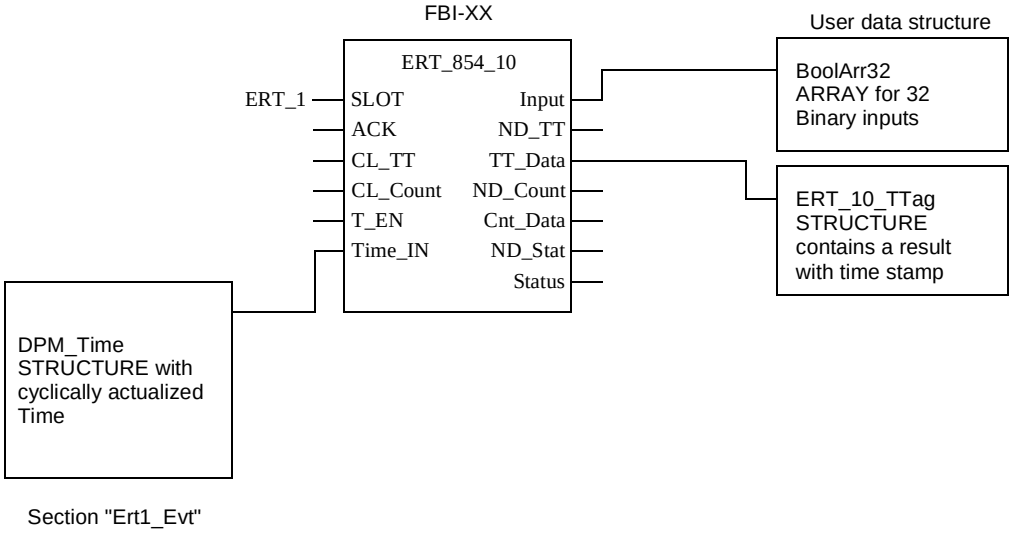
Processing Section

Processing section

The processing section for actual data processing of the ERT 854 10 EFBs.

Example

The following example of a processing section uses the parameter "slot" for its ERT_854_10 EFB which can be taken from a QUANTUM or a DROP EFB. (See also *Configuration Section, p. 67*.)
Typical implementation of an ERT_854_10 EFB in the processing section



EFBs for the140 ERT 854 10

10

Introduction

Overview

The EFBs described in this chapter are required for operating the 140 ERT 854 10.

What's in this Chapter?

This chapter contains the following sections:

10.1 DROP: Configuring an I/O station rack

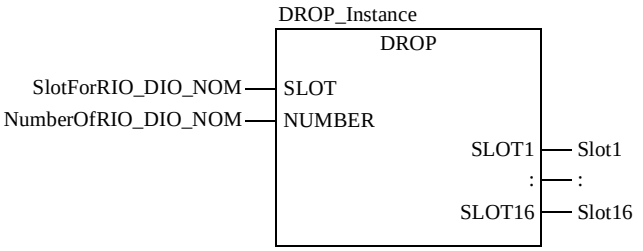
Description

Function description

The function block is used to edit the configuration data of a remote or distributed I/O station for subsequent processing by module configuration EFBs.
To configure an I/O station rack, the DROP function block in the configuration section is connected to the corresponding SLOT output of the QUANTUM function block. The number of the I/O station defined in the I/O map has to be entered at the NUMBER input of the DROP function block. The function blocks for configuration of the analog modules of the I/O stations are connected to the SLOT outputs.
EN and ENO can be configured as additional parameters.

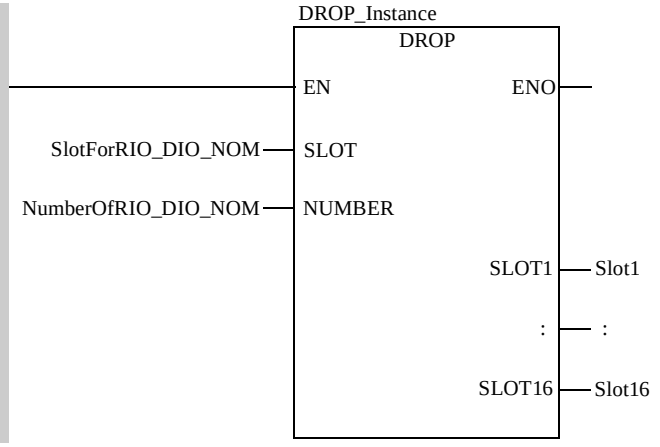
Representation in FBD

Representation:



Representation in LD

Representation:



Representation in IL

Representation:

```
CAL DROP_Instance (SLOT:=SlotForRIO_DIO_NOM,
    NUMBER:=NumberOfRIO_DIO_NOM, SLOT1=>Slot1,
    SLOT2=>Slot2, SLOT3=>Slot3, SLOT4=>Slot4, SLOT5=>Slot5,
    SLOT6=>Slot6, SLOT7=>Slot7, SLOT8=>Slot8, SLOT9=>Slot9,
    SLOT10=>Slot10, SLOT11=>Slot11, SLOT12=>Slot12,
    SLOT13=>Slot13, SLOT14=>Slot14, SLOT15=>Slot15,
    SLOT16=>Slot16)
```

Representation in ST

Representation:

```
DROP_Instance (SLOT:=SlotForRIO_DIO_NOM,
    NUMBER:=NumberOfRIO_DIO_NOM, SLOT1=>Slot1,
    SLOT2=>Slot2, SLOT3=>Slot3, SLOT4=>Slot4, SLOT5=>Slot5,
    SLOT6=>Slot6, SLOT7=>Slot7, SLOT8=>Slot8, SLOT9=>Slot9,
    SLOT10=>Slot10, SLOT11=>Slot11, SLOT12=>Slot12,
    SLOT13=>Slot13, SLOT14=>Slot14, SLOT15=>Slot15,
    SLOT16=>Slot16) ;
```

Parameter description

Description of input parameters:

Parameter	Data type	Meaning
SLOT	INT	Slot for RIO, DIO, NOM
NUMBER	DINT	Number of RIO, DIO, NOM

Description of output parameters:

Parameter	Data type	Meaning
SLOT1	INT	Slot 1
:	:	:
SLOT16	INT	Slot 16

Runtime error

If no "Head" has been configured for the I/O station rack, an error message is returned.

10.2 QUANTUM: Configuring a main rack

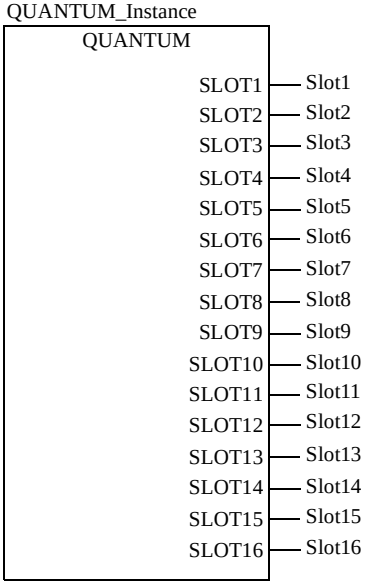
Description

Function description

The function block is used to edit the configuration data of a QUANTUM main rack for subsequent use by the scaling EFBs.
To configure a Quantum main rack, the QUANTUM function block is inserted into the configuration section. The function blocks for the configuration of analog modules or the DROP function block for the I/O station are connected at its SLOT outputs.
EN and ENO can be configured as additional parameters.

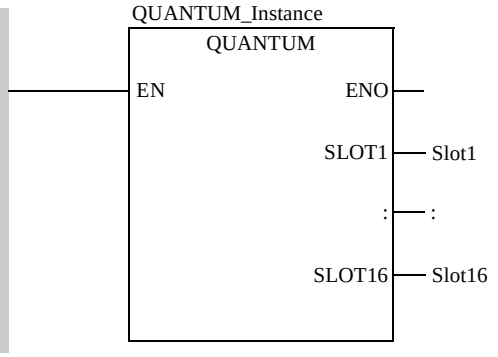
Representation in FBD

Representation:



Representation in LD

Representation:



Representation in IL

Representation:

```
CAL QUANTUM_Instance (SLOT1=>Slot1, SLOT2=>Slot2,
    SLOT3=>Slot3, SLOT4=>Slot4, SLOT5=>Slot5, SLOT6=>Slot6,
    SLOT7=>Slot7, SLOT8=>Slot8, SLOT9=>Slot9,
    SLOT10=>Slot10, SLOT11=>Slot11, SLOT12=>Slot12,
    SLOT13=>Slot13, SLOT14=>Slot14, SLOT15=>Slot15,
    SLOT16=>Slot16)
```

Representation in ST

Representation:

```
QUANTUM_Instance (SLOT1=>Slot1, SLOT2=>Slot2,
    SLOT3=>Slot3, SLOT4=>Slot4, SLOT5=>Slot5, SLOT6=>Slot6,
    SLOT7=>Slot7, SLOT8=>Slot8, SLOT9=>Slot9,
    SLOT10=>Slot10, SLOT11=>Slot11, SLOT12=>Slot12,
    SLOT13=>Slot13, SLOT14=>Slot14, SLOT15=>Slot15,
    SLOT16=>Slot16) ;
```

Parameter description

Description of output parameters:

Parameter	Data type	Meaning
SLOT1	INT	Slot 1
:	:	:
SLOT16	INT	Slot 16

Runtime error

Internal I/O map errors will cause an error message.

10.3 ERT_854_10: Data transfer EFB

Overview

Introduction

This chapter describes the `ERT_854_10` block.

What's in this Section?

This section contains the following topics:

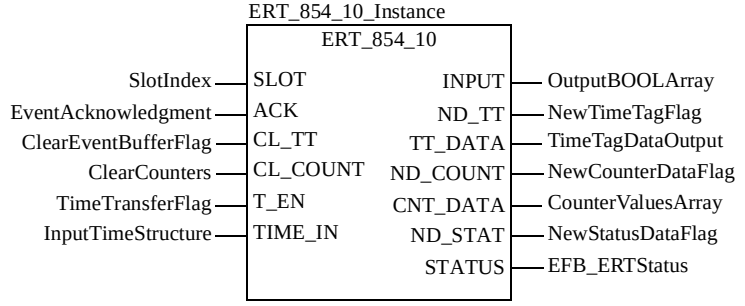
Description

Function description

The ERT_854_10 EFB provides the programmer with a software interface to the ERT 854 10 module which allows simple access of the functions such as counting, time stamp, status or time synchronization. The ERT_854_10 EFB coordinates the flow of Multiplex data from the ERT to the PLC using the input and output registers. It also ensures that the intermediate count values are put in an internal storage area until the data is complete, so a consistent set of all count values is made available to the statement list. A marker "New data" is always set for every data type if the input data type in the corresponding EFB output structure was copied.
The parameters EN and ENO can also be configured.

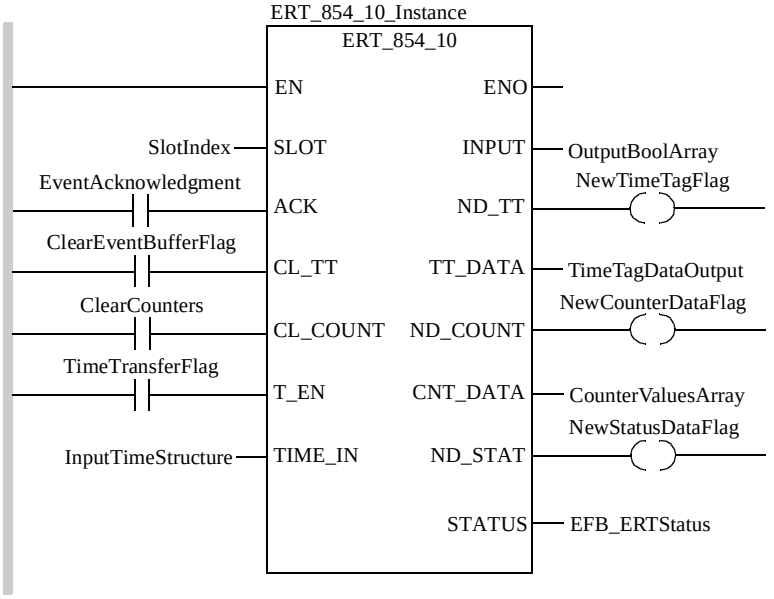
Representation in FBD

Representation:



Representation in LD

Representation:



Representation in IL

Representation:

```
CAL ERT_854_10_Instance (SLOT:=SlotIndex,
    ACK:=EventAcknowledgment, CL_TT:=ClearEventBufferFlag,
    CL_COUNT:=ClearCounters, T_EN:=TimeTransferFlag,
    TIME_IN:=InputTimeStructure, INPUT=>OutputBoolArray,
    ND_TT=>NewTimeTagFlag, TT_DATA=>TimeTagDataOutput,
    ND_COUNT=>NewCounterDataFlag,
    CNT_DATA=>CounterValuesArray,
    ND_STAT=>NewStatusDataFlag, STATUS=>EFB_ERTStatus)
```

Representation in ST

Representation:

```
ERT_854_10_Instance (SLOT:=SlotIndex,
    ACK:=EventAcknowledgment, CL_TT:=ClearEventBufferFlag,
    CL_COUNT:=ClearCounters, T_EN:=TimeTransferFlag,
    TIME_IN:=InputTimeStructure, INPUT=>OutputBoolArray,
    ND_TT=>NewTimeTagFlag, TT_DATA=>TimeTagDataOutput,
    ND_COUNT=>NewCounterDataFlag,
    CNT_DATA=>CounterValuesArray,
    ND_STAT=>NewStatusDataFlag, STATUS=>EFB_ERTStatus) ;
```

Parameter description

Description of the input parameters:

Parameter	Data type	Meaning
SLOT	INT	The Slot index is assigned to the EFB ERT_854_10 from either the QUANTUM EFB or DROP EFB and contains the configured input and output references (%IW and %MW)
ACK	BOOL	Event confirmation: Setting ACK signals that the user is ready to receive the next result and deletes the TT_DATA marker. If ACK remains set "continuous operation" appears.
CL_TT	BOOL	Delete the ERT event FIFO buffer by setting CL_TT. Saving of events is blocked until the CL_TT is reset to 0.
CL_COUNT	BOOL	Delete all ERT counters by setting CL_COUNT. Counting is interrupted until CL_COUNT is reset to 0.
T_EN	BOOL	Enables a time transfer, e.g. from the ESI using TIME_IN, if set
TIME_IN	DPM_Time	Structure of the ESI, e.g. input time through time synchronization of the ERT (carries the edge controlled time synchronization in the Sync element)

Description of the output parameters:

Parameter	Data type	Meaning
INPUT	BOOLArr32	Output field for all 32 digital inputs in BOOL format (also provided in the form of word references as %IWx and %IWx+1)
ND_TT	BOOL	Marker, new data in TT_DATA structure: remains set until user confirmation with ACK
TT_DATA	ERT_10_TTag	Event message output structure with time mark. An event is held and ND_TT is set to 1 until there is a user enable with ACK = 1.
ND_COUNT	BOOL	Marker, new counter data in CNT_DATA Structure: The value 1 is set for only one cycle and is not recorded.
CNT_DATA	UDIntArr32	Output field for 32 counter values is overwritten after the EFB has received a complete set of consistent counter values (configured as: 8, 16, 24, or 32).
ND_STAT	BOOL	Marker; new status data in STATUS word: The value 1 is set for only one cycle and is not acknowledged.
STATUS	WORD	Output word for EFB/ERT status (for internal details see *Data Flow, p. 86*)

Internal time synchronization

Structure of `DPM_Time` for ERT internal time synchronization, e.g. through the ESI:

Element	Element type	Meaning
`Sync`	`BOOL`	Clock synchronization with positive edge (hourly or on command)
`Ms_Lsb`	`BYTE`	Time in milliseconds (low value byte)
`Ms_Msb`	`BYTE`	Time in milliseconds (high value byte)
`Min`	`BYTE`	Time invalid / minutes
`Hour`	`BYTE`	Summer time / hours
`Day`	`BYTE`	Day of the week / Day in the month
`Mon`	`BYTE`	Month
`Year`	`BYTE`	Year

Event structure

Event structure of the `ERT_10_T-Tag` with 5Byte time markers (further information can be found in *Data Flow, p. 86*):

Element	Element type	Meaning
`User`	`BYTE`	Complete time / user number [module number]
`INPUT`	`BYTE`	Event set type / No. of the first input
`In`	`BYTE`	Event data: 1, 2 or 8 administered positions
`Ms_Lsb`	`BYTE`	Time in milliseconds (low value byte)
`Ms_Msb`	`BYTE`	Time in milliseconds (high value byte)
`Min`	`BYTE`	Time invalid / minutes
`Hour`	`BYTE`	Summer time / hours
`Day`	`BYTE`	Day of the week / Day of the month

Function mode

ERT data transfer

The number of I/O words available on the local and remote racks is limited to 64 inputs and 64 outputs. For this reason the number of settable ERT modules per local/remote rack with the currently selected minimum requirements of 7 input words and 5 output words is limited to 9 per module.

The size of the required ERT data transfer is considerably larger:

- 32 counters = 64 words,
- a event with a 5 byte time marker = 4 words,
- 32 digital values and the ERT status = 3 words.

These inconsistent size requirements necessitate the use of a special transfer EFB called `ERT_854_10` to execute the required operations on the PLC and to adjust the ERT representation of the data in Multiplex form. This type of EFB is required for every ERT module.

To simplify matters, configure only the EFB parameters which will actually be used. This saves on configuration, particularly when the counter inputs and event inputs get mixed with one another. Memory is not saved because Unity fills the outputs with invisib

Underlying structure of the register block

Underlying structure of the ERT_854_10 input register block with seven %IW input words for transfer from the ERT to the PLC:

Contents	Function
Digital inputs 1 ... 16	Digitally processed input data which is cyclically updated (the module's input address corresponds to that of the digital standard input modules, i.e. inputs 1 16 correspond to bits 15 0)
Digital inputs 17 ... 32	
Transfer status	IN transfer status (TS_IN)
MUX 1	Multiplex data block for block transfer, such as: ● 1 event with 5 byte time marker or ● 2 counter values of maximal configuration 32 or ● 1 status word
MUX 2	
MUX 3	
MUX 4	

Simplified structure of the ERT_854_10 output register block with five %MW output words for the transfer from the PLC to the ERT
ERT_854_10 output register block:

Contents	Function
Transfer status	OUT transfer status (TS_OUT)
MUX 1	Time data block for the ERT for the clock synchronization
MUX 2	
MUX 3	
MUX 4	

Note: User interfaces are normally the inputs and outputs of the ERT_854_10 EFB, not the %IW and %MW input/output words.

EFB configuration

EFB connection

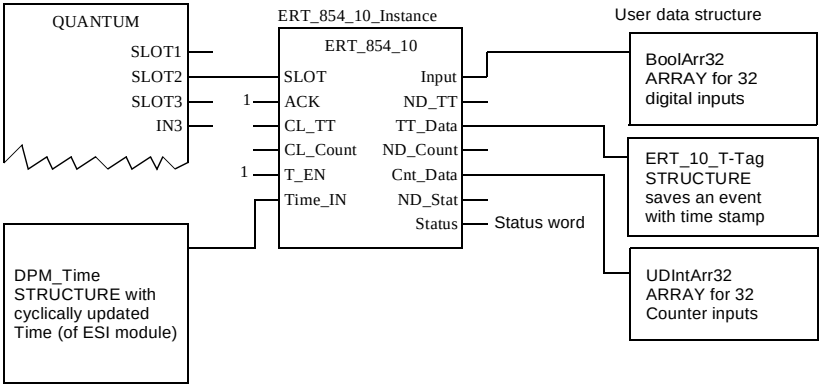
The EFB connection to the input and output references (%IW and %QW) is accomplished through a graphic connection to the ERT slot number, in the same way as with analog modules. The currently available QUANTUM and DROP EFBs from the I/O Management library are used as follows: QUANTUM for local and DROP for remote racks. These EFBs transfer an integer index to every specified slot, which points to an internal data structure with the configured values. The module parameters and the ID are stored there, in addition to the addresses and lengths of the assigned input and output references (%IW and %MW).
A significant improvement in the runtime can be achieved by deactivating the QUANTUM or the DROP EFB after the first execution.

Function of CL_TT and CL_COUNT

Setting the input marker CL_TT causes the FIFO buffer event of the ERT to be cleared. Setting the markers for one cycle is sufficient.
Setting the input marker CL_COUNT causes the ERT counter to be cleared by the ERT. Setting the markers for one cycle is sufficient.

Block diagram

Principle structure



Data Flow

Digital Inputs

No marker for new data is provided for this input type. The digital inputs in the first two input register words are updated directly by the ERT in every second cycle. The EFB makes the processed values available as Bool if the `BoolArr32` output field has been configured accordingly.

Counter Inputs

Cyclic updating of the counted values lasts significantly longer than for other data types. Counted values are saved as a data set in `CNT_DATA` after a complete series (configured as: 8, 16, or 32) of time consistent counted values in multiplex form has been transferred by the ERT. The marker for new data `ND_COUNT` is set for one cycle.

Event Inputs

Readiness to receive new events must be actively confirmed by the user, therefore the administration of markers becomes somewhat more complex (a handshake mechanism is required) Event data remain in the data structure `ERT_10_TTag` and the marker for new data `ND_TT` stays set until the `ACK` input is set and a new event thus requested. The EFB responds to this by resetting `ND_TT` for at least one cycle. After the new event has been sent to the ERT_10_TT structure (marker structure), `ND_TT` is reset by the EFB. To prevent the new event data from being overwritten attention must be paid to fundamentally resetting the `ACK` input after the EFB has reset the `ND_TT` marker. This state can then remain stable to allow the user program enough time for event processing. Each subsequent event tracked with the ERT is temporarily stored within the event FIFO buffer.
New events are sent directly from the internal buffer of the EFB in intervals of at least 2 cycles for as long as the `ACK` input is set (for the special continuous operating mode); the effect is, however, that the `ND_TT` only stays set for one cycle. In this special mode the user program's task is still to terminate event processing before `ND_TT` signals the transfer of other new events to the ERT_10_TT structure as handshake protection by `ACK` is not available in this case.

ERT_10_TTag ERT_10_TTag event structure with 5 byte time marks

Byte	Bits	Function
1	D0...D6 = Module no. 0...127 D7 = CT	Rough time: CT = 1 indicates that this time mark contains the whole time declaration including month and year in bytes 2 + 3. The Module no. can be set in any way in the parameter screen.
2	D0D5 = input no. D6 = P1 D7 = P2	No. of the first input of the event group: 1...32 Type of the event message (P2, P1). 1..0.3 see *Note 1:, p. 87* [Month value with CT = 1]
3	D0D7 = data from the event group (D7D0 with right alignment)	1, 2 or 8 managed positions [year value, if CT = 1]
4	Time in milliseconds (low value byte)	0 ... 59999 milliseconds (max. 61100) see *Note 2:, p. 88* and *Note 3:, p. 88*
5	Time in milliseconds (high value byte)	
6	D0...D5 = minutes D6 = R D7 = TI	Minutes: 0...59 Time invalid: TI = 1 means invalid time / reserved = 0 see *Note 3:, p. 88*
7	D0...D4 = hours D5 = R D6 = R D7 = DS	Hours: 0...23 Summer time: DS = 1 indicates that summer time is set With shift SZ -> WZ has hour 2A and id SZ, and hour 2B has id WZ
8	D0...D4 = DOW D5...D7 = DOM	Weekday: Mon-Sun = 17 Day of the month: 1...31 The id corresponds to CET and thus deviates from the standard used in the US, Sun = 1.

Note 1: Interpretation for byte 2

D7 D6	Type of event message	D5...D0	No. of the first input of the event group
0 1	1 pin message	1 ... 32	Input pin number
1 0	2 pin message	1, 3, 5, ...31	First input of the group
1 1	8 pin message	1, 9, 17, 25	First input of the group

Note 2: The value for the milliseconds is a maximum of 61100 ms with switch seconds (61000 plus a tolerance of 100 milliseconds)

Note 3: For time markers containing an invalid time (TI = 1), the time in milliseconds is set to FFFF HEX. Minutes, hours and DOW/DOM values are invalid (i.e. undefined).

Rough time declaration If the "rough time declaration" has been activated during the ERT configuration, the transfer of the complete time (with month/year) is executed in the following conditions: when the month changes, after the module restarts, during every start or stop of the PLC user program, when the event FIFO buffer is deleted, when the clock is started or set. If this rough time declaration is sent without the data input values, "triggering" basically takes place through a correct time stamped event. If this does not happen the values remain "stuck" in the ERT until an event occurs. Within the time mark of a "rough time declaration", the CT bit is always set so that byte 2 contains the information about the month, byte 3 the information about the year and bytes 4 to 8 display the same time mark values of the triggered event whose event message appears immediately after the rough time declaration.

Status Inputs The marker for new status data `ND_STAT` is set for one cycle. The status inputs can be overwritten after 2 inquiry cycles.
The status word contains EFB and ERT error bits

Division of the Error Bits Internal structure of the EFB/ERT status word:

EFB error bits					**ERT error bits**										
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

ERT Error Bits

D8 ... D0 ERT error bits

Bit	Brief designation	Meaning
D0	FW	Firmware errors, self test errors within EPROM, RAM or DPM (severe module errors)
D1	FP	Parameterization errors (severe internal errors)
D2	TE	external time reference error (time-basis signal disrupted or not present)
D3	TU	Time became invalid
D4	TA	Time is not synchronized (Free run mode, permanent run without time error message, see also:*Without power reserve, p. 92*
D5	PF	FIFO buffer overrun (loss of the most recent event data)
D6	PH	FIFO buffer half full
D7	DC	Stabilize active (some event data lost)
D8	CE	ERT communication errors (procedure errors or time out)

When configuring the parameter screen some of these errors can be assigned to grouped error messages with the "F" light as well as the module's error byte within the status table. All other errors are then defined as warnings.
D11 ... D9 reserved

EFB Error Bits

D15 ... D12 EFB error bits:

Bin.	Hex	Meaning
1000	8 HEX	EFB communication time out
0101	5 HEX	Wrong slot
0110	6 HEX	Health status bit is not set (ERT appears as not available)
Other values		Internal error

Online error display

The following ERT/ERB error messages are displayed in the **Tools** → **Diagnostic Display** UNITY window with an error number and explanation.
EFB error messages:

Message	Error	Meaning
-30210	User error 11	EFB communication time out
-30211	User error 12	EFB internal error
-30212	User error 13	EFB internal error
-30213	User error 14	EFB internal error
-30214	User error 15	EFB internal error
-30215	User error 16	Wrong slot
-30216	User error 17	Health status bit is not set (ERT appears as not available)
-30217	User error 18	EFB internal error

ERT error messages:

Message	Error	Meaning
-30200	User error 1	ERT internal error
...	...	...
-30207	User error 8	ERT internal error
-30204	User error 5	ERT communication timeout (e.g. EFB too long disabled)

Other Functions

Input marker

Setting the input marker `CL_TT` deletes the Event FIFO buffer of the ERT. Setting the marker for one cycle is sufficient.
If the input marker `CL_Count` is set, the ERT counter is deleted by the EFB. Setting the marker for one cycle is sufficient.

Use of the DPM_Time structure for the synchronization of the internal ERT clock

Time synchronization

If the time cannot be synchronized through a standard time receiver, the time information can alternatively be transferred from the 140 ESI 062 01 communication module. The ESI makes the updated time available directly to the EFB in a DPM_Time structure via the TIME_IN parameter. The data structure can also be filled by the user program and the respective bits can be managed. In this way, for example, the time can be set by the CPU.

With power reserve

As soon as the "clock" parameter of the ERT is configured as an "internal clock" with a power reserve not equal to zero (i.e. not free running) the EFB must use the time supplied by the ESI for the synchronization of the internal ERT clock. Until the first synchronization has taken place, the ERT sends back the set Bit "invalid time" in the STATUS output word (Bit 3 TU).
The conditions for the first synchronization of the internal ERT clock via the DPM_Time structure are:
The EFB Parameter T_EN must change from 0 to 1 to enable the time setting.

The time in TIME_IN made available by ESI must look as follows:

- valid (i.e. the bit for the message "time invalid" in Min value must not be set),
- and the values in Ms must change continually.

Should the time data later become invalid or no longer set, then the TU does not switch to 1 until the configured power reserve has expired.

The synchronization/setting of the internal ERT clock takes place via the DPM_Time structure, if:

- EFB-Parameter T_EN is set to 1 to enable the time setting.
- The time data in TIME_IN made available by ESI are valid (i.e. the "Time invalid" Bit in the Min value must not be set).
- The status of the DPM_Time element Sync changes from 0 to 1. This change is run every full hour by the 140 ESI 062 01 but can also be performed as the result of a suitable telecontrol command.

The precision of the time synchronized by the ESI at the ERT can be influenced by delays, by the PLC cycle time, as well as by the cumulative component, which reflects the differences in the ERT software clock (< 360 milliseconds/hour).

Without power reserve

If the "clock" parameter of the ERT was configured as an "internal clock" in free running mode (with a power reserve of zero), the internal clock starts with a default setting at hour 0 on 1/1/1990. In this case the time can also be provided by using the DPM_Time data structure of the 140 ESI 062 01 module, as described above. As there is no power reserve available for use, the time will never be invalid and the Bit "Time not synchronized" within the STATUS output word (Bit 4 TA), given back by the EFB, is always set.

Using the ERT >EFB Time Data Flow

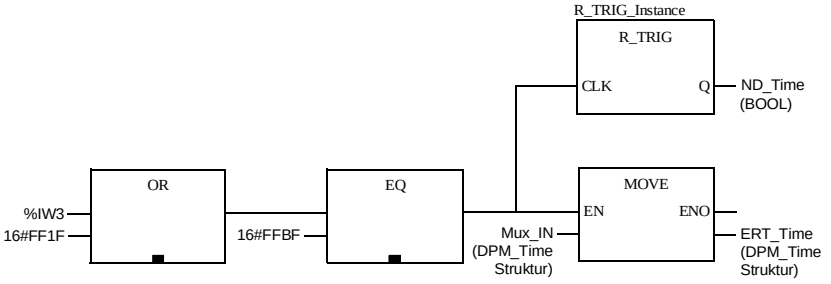
Application examples

This section presents an internal function which is made available through the ERT for diagnostics and development. It covers the cyclic transfer of the ERT internal time to the corresponding EFB in greater intervals. This time application can be used to display or set the PLC clock etc, regardless of whether it comes from the free-running internal clock or was synchronized through an external reference clock signal. The time appears as a `DPM_Time` structure beginning with word 4 of the IN register block of the ERT. The following diagram shows the program elements involved in selection.

Commissioning information

A `ERT_854_10` was assigned the IN references %IW1 ... . %IW3 during I/O addressing. The IN transfer status (TS_IN) in the third word of the register block is sent to an OR block. A `DPM_Time` structure is defined within the variable editor as Variable Mux_IN in the fourth word of the IN register block, and therefore has the address %IW4 ... %IW7. This variable is sent to the `MOVE` block as an entry. The `MOVE` block output is a `DPM_Time` structure defined by the variable editor as variable `ERT_Time`.

Typical recording mechanism for ERT time data



Note: The `ERT_854_10` EFB must be active and error free.

Explanation:

The `MOVE` block transfers the time data cyclically stored in the MUX zone of the IN register block to the `DPM_Time` structure `ERT_Time` belonging to the user as soon as the `OR` and the `EQ` block signals a time data transfer. `R_TRIG` makes a signal in `ND_Time` available for further processing of the time data available for one cycle. The `BOOL Sync` element value of the `ERT_Time` should begin to "tick" during each new transfer from the ERT. There is a new transfer after a maximum of each 200 PLC cycles.

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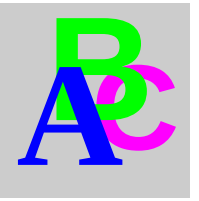

Numerics

A

B

C

D

E

F

G

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P

Q

R

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V

W